ABSTRACT OF THE DISCLOSURE

DUAL CACHE DIRECTORIES ALLOWING SIMULTANEOUS READ OPERATIONS

A method of accessing values stored in a cache used by a processor of a computer system, whereby two read operations may occur simultaneously is disclosed. Memory blocks from a memory device are loaded into respective cache lines of the cache, and address tags associated with the memory blocks are written into two redundant cache directories of the cache. Thereafter, a first memory block can be read from the cache using the first cache directory, while a second memory block is simultaneously read from the cache using the second cache directory. The cache can have a single cache entry array, or two (redundant) cache entry arrays connected respectively to the two cache directories. If an error occurs when examining a particular address tag in one cache directory, then a redundant address tag can be substituted for the particular address tag by examining a corresponding line of the other cache directory.